

# Rapid Parallel GPS Signal Acquisition

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## BIOGRAPHY

**Ville Eerola** was born in Finland. He has received the degree of Diploma Engineer in electrical engineering from Tampere University of Technology in 1990. He has worked at VLSI Solution since 1992. He has been involved in GPS receiver technology development since 1992. His research interests include spread spectrum communications and signal processing in communication systems. He is a co-founder of VLSI Solution Oy.

## ABSTRACT

A GPS acquisition system which achieves extremely short search times is presented. The system requires no prior knowledge of position or time. Using a 50 MHz clock frequency, 25 satellites can be searched in parallel. Under nominal signal conditions, two-second search times have been demonstrated. The acquisition unit performance has been verified both with live satellites as well as with a GPS simulator. With the GPS simulator the performance with weaker signal conditions was also evaluated. The acquisition threshold was found to be  $-134$  dBm with a RF noise figure of 4 dB.

The developed acquisition system is based on parallel matched-filter implementation, which is capable of searching code offsets of a number of satellites simultaneously. The frequency domain is searched by sweeping a common local oscillator frequency. The search process is controlled by a state machine, which has a number of parallel channels, each capable of performing a search of its corresponding PRN code. This implementation is considerably more effective than performing sequential search of each satellite signal. The modest hardware complexity increase and the search speed improvement compared to the single-satellite search unit makes the parallel architecture attractive.

The advances in current CMOS manufacturing technologies make fully digital implementation of a matched filter based acquisition unit economically possible even for low-cost GPS receivers. The acquisition system has been implemented in  $0.35\ \mu\text{m}$  CMOS process. A sensor GPS receiver containing the acquisition unit, 12 channel corre-

lating receiver together with the DSP and SRAM memory for running the tracking algorithm fits in a single chip and is packaged in a 64-pin LQFP package.

## 1. INTRODUCTION

An important design parameter for GPS receivers is the Time To First Fix (TTFF). In usual GPS applications, the receiver has some knowledge of its location, the current time, and the approximate satellite orbit parameters. It can use this information to aid in the initial signal search. If this information is not available, the carrier frequency search should cover at least the full Doppler uncertainty, the code phase search should cover all 1023 chips, and all possible satellites should be searched for. This kind of search can take several minutes to perform without aid of special hardware.

The full sky search problem has been an uninteresting area for many GPS receiver designers because of its infrequent need, as the location, the current time, and the approximate satellite orbit parameters are usually available. However, there are some applications where providing this information would be hard or uneconomical. For example, the GPS receiver can be used as a sensor for determining location and speed of an object which is destroyed or lost after each use. In such case the receiver needs to be small, self-contained, low-cost, and usually has no way of uploading any information to it prior usage. In many cases, the signal acquisition speed is critical for successful operation. This kind of sensor receivers usually operate in differential mode where a base station with a continuously operating GPS receiver performs the differential position computations. Thus, only the time-stamped receiver measurements are needed for proper operation, and the cold-start time is not restricted by time required to receive the ephemerides.

The developed acquisition unit described in this paper is for C/A-code GPS receivers aiming for rapid signal acquisition when no information on the location, time, and satellite orbits are available for the receiver, and which need acquisition of signals from at least 4 satellites within a couple of seconds from turning on the receiver. The sensitivity of the acquisition process was not critical in this application,

as the receiver is to be used in open sky environment. The acquisition unit is based on parallel matched-filter implementation, which is capable of searching code offsets of a number of satellites simultaneously. The advances in current CMOS manufacturing technologies make fully digital implementation of a matched-filter-based acquisition unit economically possible even for low-cost GPS receivers. The application for which the presented acquisition unit was developed is cost sensitive, but it still requires high signal acquisition speed, which makes the described architecture well suited for it.

The acquisition unit is a part of a full GPS receiver baseband chip with the acquisition unit, 12 channel correlating receiver together with the DSP and SRAM memory for running the tracking algorithm. The block diagram of the chip is shown in Fig. 1. The receiver is intended to be used in differential configuration where a base station with a continuously operating GPS receiver performs the differential position computations. The receiver chip does not have enough memory to run the full navigation processing. The receiver still requires a proper signal tracking to achieve the required measurement accuracy, as the matched filter can measure the code offsets with only about one-chip accuracy. The whole receiver baseband fits in a single chip and is packaged in a 64-pin LQFP package and has been implemented in a 0.35  $\mu\text{m}$  CMOS process.

## 2. MATCHED FILTERS

Matched filters [1] are devices which continuously compute correlation between a known (reference) signal and a signal to be measured, and give maximal output when the correlation between the reference signal and the incoming signal is strongest. They can be implemented either as a continuous time or discrete time operation. By definition, they are optimum detectors for signals embedded in additive white Gaussian noise (AWGN). Thus a matched filter (MF) is a useful device to be used in the acquisition phase of spread spectrum receiver operation to search the correct timing for the replica code.

The bandpass matched filter is implemented using the low-pass equivalent format for bandpass filters (Fig. 2). The implementation of a matched filter for finite-length pseudo-random-number (PRN) waveform is most easily visualized in the form of a tapped delay line followed by a passive filter matched to a *single* PRN waveform as illustrated in Fig. 3. The output filter ( $P^*(\omega)$ ) is matched to the basic pulse shape of the PRN spreading chips. In the case of rectangular chips it can be ignored.

## 3. ALGORITHM

The basic operation of the MF acquisition system is as follows: The incoming samples are multiplied by sine and cosine signals produced by a numerically controlled oscillator (NCO). The frequency of the NCO is equal to the GPS

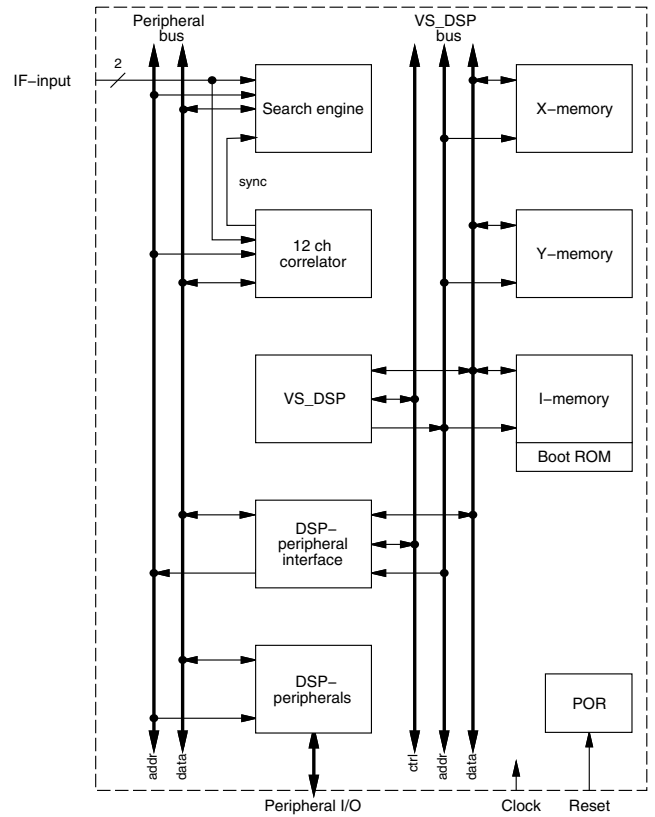


Figure 1: Block diagram of the GPS receiver baseband chip.

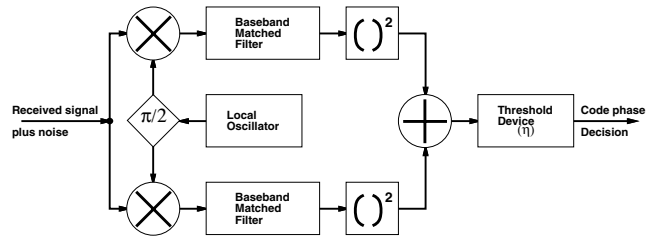


Figure 2: A band-pass version of a matched filter acquisition system using low-pass filters.

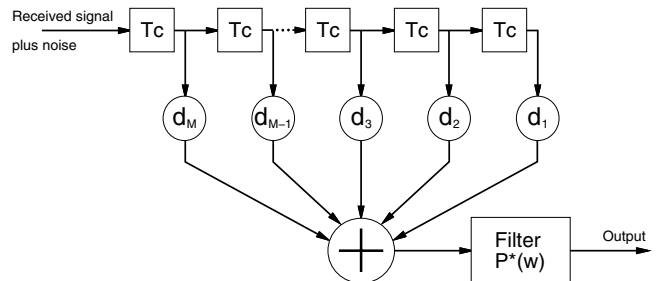


Figure 3: A tapped delay line implementation of a matched filter for an M-chip PRN sequence.

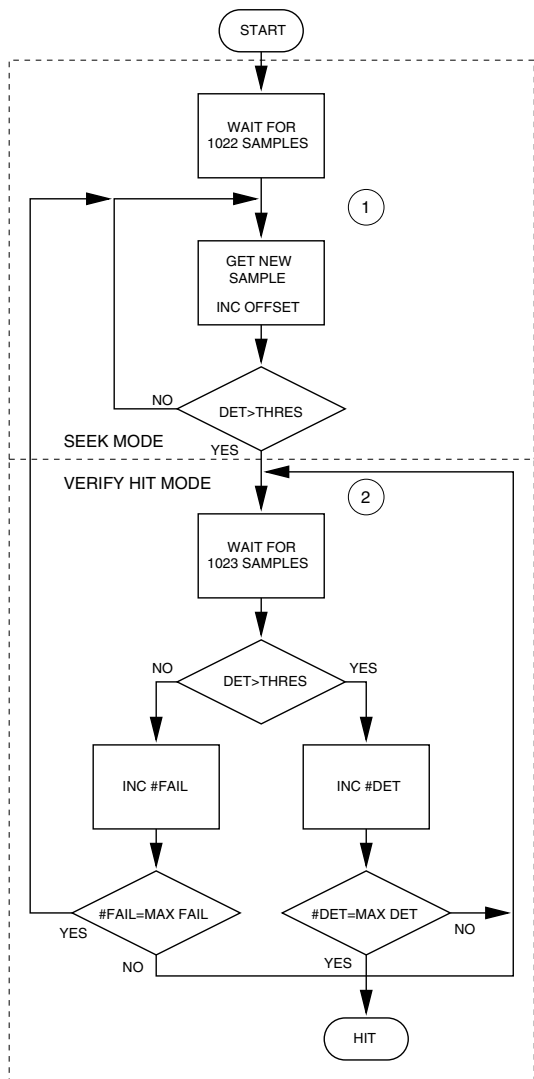


Figure 4: Flowchart of the MF search algorithm.

satellite Doppler plus the intermediate frequency (IF). The detection and verification process is performed independently for each PRN signal. The flowchart of the acquisition process is shown in Fig. 4. The used algorithm implements an M out of N majority logic decision with early termination.

In the first step the shift register is loaded with data from the input block one sample at a time. As the length of the matched filter is 1023 samples, we need to load 1022 samples at this stage. In the next step (1) one more sample is loaded into the shift register. Now, the data in the shift register is compared to the reference PRN signal in the matched filter. If the threshold is not exceeded, we go back to point (1) and load the next input sample. If the comparison value exceeds the set detection threshold, a potential match is noticed. In the simplest case exceeding the threshold would mean that the signal has been found, and its code phase is aligned with the reference signal in the

matched filter. However, in most practical cases the signal to noise ratio of the received signal is too low to get a reliable detection on single comparison. To increase the detection probability and decrease the probability of false detection a number of verification comparisons are done. So, if a possible hit was found, the system enters verification mode at point (2). There the shift register is first loaded with 1023 fresh data samples to improve detection statistics and to arrive at the same code phase position. After the wait, the threshold comparison is repeated. If the threshold is not exceeded, the value of the *fail* counter is incremented. The counter is compared against a set maximum value, which sets a limit on failed verification comparisons. If the value of the counter reaches the limit, the verification is considered as failed and the search is continued in search mode by loading the next input sample at point (1). Otherwise, the verification step is repeated by going back to point (2). If the comparison value is above the threshold, the value of the *det* counter is incremented. The counter is then compared against a set maximum value, which sets a limit on successful verification comparisons. The signal is declared as found if the value of the counter equals to the limit and the search ends. Otherwise we go back to point (2) to repeat the verification.

The maximum values for the *fail* and *det* counters set the limit of total verification rounds to the sum of the limits plus one. The optimization process for the limits is described in more detail in [1]. The threshold value selection process needs to consider the desired detection and false alarm probabilities. One method for this is presented in [2].

After checking all possible code offsets for all the parallel channels, the NCO frequency is increased by a given value, and if it is not above the maximum value, the search process is repeated. When the frequency reaches the maximum value, it is set to the starting value, the set of PRN sequences to be used is changed, and the search starts from the beginning. Waiting for all channels to check all possible code offsets means that some of the channels may in fact search each frequency bin more than once, and the time between frequency sweeps depends on the slowest channel getting all of the code phases checked.

#### 4. HARDWARE

The MF acquisition system implements a parallel matched filter with integrated search control. The user only needs to configure the main search parameters such as the frequency and detection limits, and the MF acquisition system independently searches the whole uncertainty space. The results of the search are reported to the user through the DSP interface.

The MF acquisition system implements the 25 parallel channels in a time-shared manner. The limit in the number of channels comes from the ratio of the master clock fre-

quency to the required sampling frequency of the MF. In this case the ratio is 50. The single MF core processes both in-phase and quadrature versions of each channel, reducing the number of possible channels to 25. Since the number of possible channels is smaller than the total number of possible PRN sequences to search, the PRN sequences being searched must be changed periodically. The PRN signals to be checked are stored in a ROM, and the time-multiplexing of the reference signals is done by incrementing an address counter for the ROM. The counter counts from a base address up 25 times modulo 32. The change of the set of PRN signals to be searched is done by changing the base address, which is done after sweeping through all frequencies to be searched. The base is changed by a configurable increment, which is again counted modulo 32. The configurable base increment allows for tuning the search process.

There are several events within the MF, which generate output allowing the user to be aware of the search progressing. The generated event types are:

**PRN Found** In this case the search was successful. The found counter exceeded the preset maximum value. The PRN number, code phase offset, frequency and hit/failure statistics are available for the user.

**Not Found** In this case the search was not successful. The failure counter exceeded the maximum value. The PRN number, code phase offset, frequency and hit/failure statistics are available for the user.

**Next Frequency** This is to inform that all 25 PRN channels have checked every code phase offset, and the frequency is incremented by the given value. The new frequency is available for the user.

**Next Base** This is to inform that all 25 PRN channels have checked every frequency, and the base is incremented by the given value. This event occurs at the same time than the last frequency sweep event, and they are combined into one data packet.

The events reported to the user can be configured by using the MF configuration register. The only event that is always reported is the *PRN found* event.

The architecture of the GPS acquisition system is shown in Fig. 5. The top level is composed of four blocks: the datapath, which contains the actual matched filter implementation; the control block, which generates the necessary control signals for the other blocks; the state machine controlling the search algorithm; and the I/O block interfacing the MF to the on chip bus.

#### 4.1. Datapath

The matched-filter datapath block contains the MF datapath proper, the MF input processing block, the ROM address generation unit, and the local oscillator NCO. The

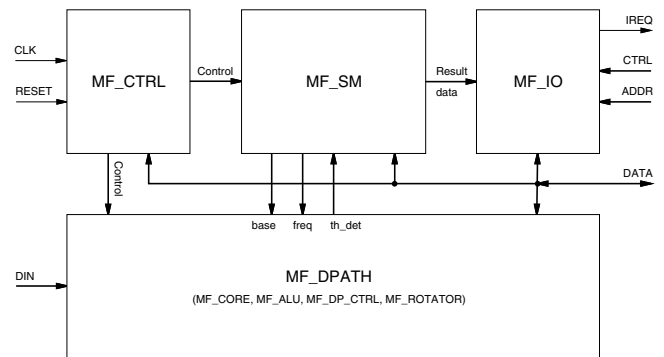


Figure 5: Block diagram of the MF unit.

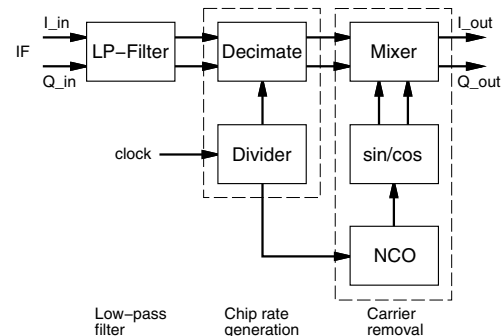


Figure 6: Block diagram of the MF input processing block.

MF input block, illustrated in Fig. 6, contains a complex low-pass filter, a decimator, an IF local oscillator, and an IF mixer. The IF mixer performs the complex multiplication of the input signal by a locally generated carrier replica signal to remove the Doppler residual. The input processing consists of decimation of the 1-bit input signals from the original sampling rate of 51.15 MHz and rotating the complex signals phase with sine and cosine local oscillator signals produced by the NCO. The NCO runs at the MF sample rate (1.023 MHz) and has 16-bit frequency resolution ( $\approx 15.6$  Hz).

The matched-filter datapath, shown in Fig. 7, is the core of the whole matched-filter acquisition system. The MF design is of the low-pass type and the datapath arithmetic is time-multiplexed to process both the in-phase and the quadrature channels. The matched-filter length in this implementation is 1023 samples, corresponding to the full PRN code length. The incoming 1-bit I- and Q-data streams are loaded into two parallel shift registers and matched against the reference signals stored in a ROM. The ROM addresses are generated by an address generation unit, which enables the MF to process multiple PRN searches in parallel by time-multiplexing the used reference signals. The data and the reference signal values are compared by an XNOR gate whose output is one if its two inputs are the same. The single MF tap implementation has two shift-registers bits for the input data streams, and a

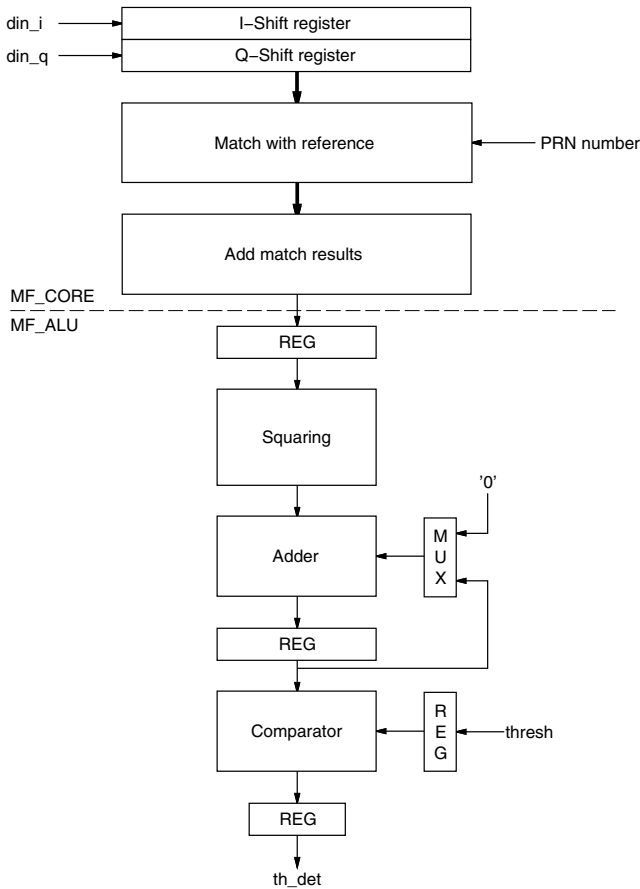


Figure 7: Block diagram of the datapath of the MF search engine.

32 by 1 ROM for holding the reference PRN signals. The data registers are compared to the reference PRN data with an XNOR gate. The comparisons are done in alternating order, i.e. first the I-channel data, and the the Q-channel data.

After the comparison, 1023 data values of 1-bits each need to be added together for every sample to produce the output of the MF. This is the most challenging part of MF implementations. Adding together the 1-bit comparison results gives the number of successful comparisons. However, it is possible to have a total match of the PRN code to the input signal, with just the sign of the input data reversed. In this case we get zero successful comparisons. In fact, the worst case match occurs when exactly half of the comparisons are wrong. To accommodate this we need to get a result that is signed and whose values are between plus and minus half of the MF length (-512 to +511).

After adding the compared bits and subtracting the offset, a pipeline register holds the result before squaring. The squared MF results are added together two at a time to combine the I- and Q-branch MF results. The combined result is finally compared by a configurable threshold value,

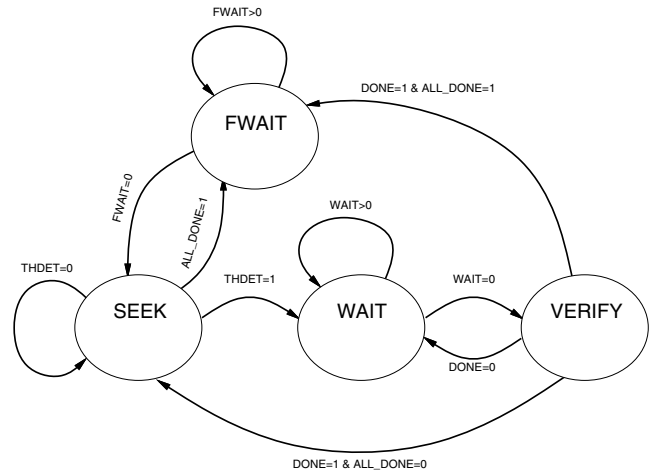


Figure 8: State diagram of the MF state machine.

and the comparison result is the output of the MF datapath.

#### 4.2. The State Machine

The MF state machine is responsible for the high level search control of the MF. It implements 25 parallel operating state machines, each responsible for search of one PRN signal. The operation of the state machine channels is independent except for the synchronization of frequency and PRN base addresses, which happens only when each of the channels have processes all of the possible PRN code phase offsets once.

One channel of the MF state machine is illustrated in Fig. 8. There are two active states and two states used for waiting. The starting state is the **fwait** state, in which new data is clocked into the shift-registers. The wait in this state lasts for as many sample clock cycles as there are bits in the shift register. After the sweep wait the **seek** state is entered. While in this state the threshold detector output is checked on every sample, and if the threshold was exceeded the next state, **verify wait** state, is entered, the *hit* counter is set to one, and the *fail* counter is set to zero. If the last code offset was reached, the state machine sets the *done* flag for the current PRN channel. When all the state machine channels have checked every possible code phase offset, i.e. when all the *done* flags are set, the frequency is swept, optionally the PRN address base register is updated, and the **fwait** state is entered.

In the **verify wait** state the state machine waits for the data shift register to shift in totally new data in order to improve the detection statistics, and to reach the same code offset position. In order to verify the satellite detection, the threshold comparisons are repeated multiple times at the same code offset position. After waiting in the **verify wait** state for the length of the PRN sequence, the **verify** state is entered. In this state, the threshold detector value is checked, the *hit* or *fail* counter is incremented. If the num-

ber of hits and fails are still below their respective maximum values, the **verify wait** state is entered again. If the number of hits is above the maximum value, a satellite signal is declared as found. After the last verify, if the code offset is the last one, the **done** flag is set and the **fwait** state is entered if all the flags are set. Otherwise, the **seek** state is entered again, and the search continues normally.

The MF state machine sweeps the frequency between the low and high limit values by configurable steps. The frequency is the fixed IF plus the satellite Doppler frequency, so the limits should be set according to the real RF front-end IF and the largest expected Doppler shift. In addition, the *hit* and *fail* counter limits can be configured through a configuration register. There is also a mechanism for initializing the MF system to its initial state. The code offset used in reporting is relative to the local clock counter of the GPS receiver chip.

## 5. ADVANTAGE OF PARALLELISM

The MF-based implementation provides orders of magnitude improvement over traditional serial-search based on correlator implementations as it is equivalent to a set of correlators operating in parallel.

To evaluate the advantages of parallel MF acquisition unit, a set of simulations has been performed. The simulations were run with varying number of PRN codes searched simultaneously. The results of the simulation are shown in Fig. 9, which shows the search overall time versus the number of parallel channels for two threshold value settings. Using the higher threshold value increases acquisition speed as can be expected. It can clearly be seen that even using only two parallel channels improves the acquisition speed dramatically. The total search time is almost half of the search time for single PRN code at a time. The advantage levels off when more channels are added, but the optimum is to search all possible codes simultaneously. The two lines show acquisition times for different threshold values and it can be seen that the relative advantage is similar independent of the threshold values.

To get another view of the same simulation Fig. 10 shows the search time of a single frequency for one set of parallel PRN codes (solid line). It shows that the time to go through all possible code phases increases with the number of parallel channels. However the time required for each PRN code decreases as shown as the dashed line. This means that this implementation is less effective than a number of parallel, completely independent search channels. However, it is still considerably more effective than performing sequential search of each satellite signal. The modest hardware complexity increase and the search speed improvement compared to the single-satellite search unit makes the parallel architecture attractive.

The acquisition unit performance has been verified both

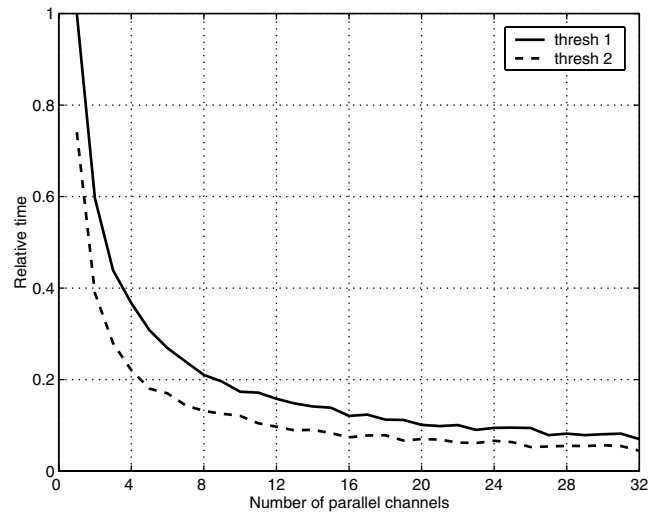


Figure 9: Relative acquisition times versus number of channels.

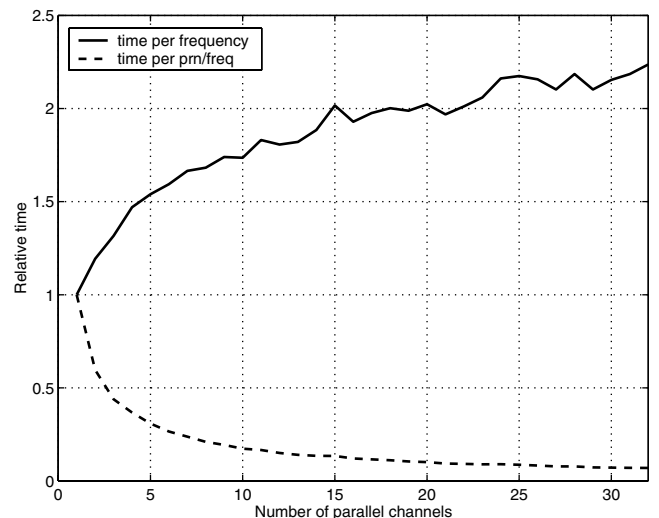


Figure 10: Relative acquisition times for one frequency sweep versus number of channels.

with live satellites as well as with a GPS simulator. Under nominal signal conditions, two-second total search times have been demonstrated. This includes two frequency sweeps with 25 PRN codes each. With the GPS simulator the performance with weaker signal conditions was also evaluated. The acquisition threshold was found to be  $-134$  dBm with a RF noise figure of 4 dB.

## 6. CONCLUSIONS

A rapid GPS acquisition system requiring no prior knowledge of position, time or almanacs was presented. The system operates autonomously, and is based on a parallel matched-filter structure. The system has been implemented in CMOS and is used as a building block for a GPS-based sensor application. The acquisition speed has

been found to be excellent. The MF-based implementation provides orders of magnitude improvement over traditional serial-search based on correlator implementations. Furthermore, the parallel MF architecture offers a significant acquisition speed improvement over a single-PRN search approach.

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